# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/788,725 | 02/26/2004 | Michael W. Morrow | MP1439 | 6814 |

22852      7590      01/10/2007

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| EXAMINER |
|---|
| KIM, HONG CHONG |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/10/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 10/788,725 | MORROW, MICHAEL W. |
| | Examiner | Art Unit | |
| | Hong C. Kim | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on <u>20 December 2006</u>.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) <u>1,2,4-8 and 10-29</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1,2,4-8 and 10-29</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**Detailed Action**

1.      Claims 1-2 and 4-8, 10-29 are presented for examination.   This office action is in

response to the RCE filed on 12/20/06.


### Information Disclosure Statement

2.      Applicants are reminded of the duty to disclose information under 37 CFR 1.56.


### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.      Claims 1, 2,  4, 5, 10-21, and 26-29 are rejected under 35 U.S.C. 102(e) as being

anticipated by Hironaka et al. (Hironaka) US Patent Pub. No. 2004/0088489.

As to claim 1, Hironaka discloses a storage device, comprising: a cache array

having cache lines filled with contiguous instructions in an instruction cache (ICache)

portion (Fig. 11 Ref. 30 and Fig. 14) that is adjacent to a trace cache (TCache) portion

where cache lines are filled with elements of a trace (Fig. 11 Ref. 30); and neither the

ICache portion nor the TCache portion is looked-up when the TCache portion is

supplying instructions (blocks 19, 20, and 147, executing series of instruction strings, "pseudo basic block" in a trace cache is read on this limitation since if there a trace cache hit, traced instructions in the trace cache are continuously accessed in a string fashion) and an instruction indexing logic, wherein the indexing logic is not used for either the ICache portion or TCache portion when the Tcache portion is supplying instructions (block 20, executing series of instruction strings, "pseudo basic block" in a trace cache is read on this limitation since if there a trace cache hit, traced instructions in the trace cache are continuously accessed in a string fashion without using any indexing logic however if there is a trace cache miss, instruction is fetched from a instruction cache utilizing a fetch address).

As to claim 2, Hironaka further discloses wherein the ICache portion is looked-up using the indexing logic when the TCache portion is not supplying instructions (block 20).

As to claim 4, Hironaka further discloses a line in the TCache portion is indexed when a branch instruction is executed (Fig. 11 and Fig. 13).

As to claim 5, Hironaka further discloses the TCache portion contains non-contiguous instructions from an instruction stream (Fig. 11, branch predictor read on this limitation since a branch address is not sequential, see Fig. 14).

As to claim 21, Hironaka further discloses wherein the ICache and TCache portions may migrate within the cache as time progresses (block 14, storing a sting of instructions is stored in the trace cache reads on this limitation).

As to claim 10, Hironaka discloses a method, comprising: intermingling cache lines in one array of a cache where a first cache line in a trace cache (TCache) portion (Fig. 11 Ref. 30) is physically adjacent a second cache line in an instruction cache (ICache) portion (Fig. 11 Ref. 30 and Fig. 14) and selecting the TCache or the ICache portion based on an address of the next instruction (Fig. 13, hit judgment circuit ) and using an instruction indexing logic to select some instructions wherein the indexing logic is not used for either the ICache portion or TCache portion when the Tcache portion is supplying instructions (blocks 19, 20, and 147, executing series of instruction strings, "pseudo basic block" in a trace cache is read on this limitation since if there a trace cache hit, traced instructions in the trace cache are continuously accessed in a string fashion without using any indexing logic however if there is a trace cache miss, instruction is fetched from a instruction cache utilizing a fetch address). .

As to claim 11, Hironaka further discloses dynamically changing a number of lines in the ICache portion and the TCache portion (Fig. 11 Ref. 30, instruction/trace integrated cache reads on this limitation).

As to claim 12, Hironaka further discloses dynamically altering a size of the ICache portion and the TCache portion in the one array as time progresses (Fig. 11).

As to claim 13, Hironaka further discloses supplying a program-order stream of instructions from each cache line in the TCache portion (Figs. 11 and 14, instruction cache).

As to claim 14, Hironaka further discloses supplying instructions in program order from cache lines in the ICache portion until a branch is encountered (Figs. 11 and Fig. 14).

As to claim 15, Hironaka further discloses associating a next address with the first cache line in the TCache portion to allow a next line to be ready before a current line is completely fetched (block 7. parallel processing).

As to claim 26, Hironaka further discloses wherein the ICache portion is looked-up using the indexing logic when the TCache portion is not supplying instructions (block 20).

As to claim 27, Hironaka further discloses wherein the TCache line size is a multiple of the (Cache line size (block 20, fetch from Icache when there is a Tcache miss reads on this limitation).

As to claim 28, Hironaka further discloses wherein the ICache and TCache

portions may migrate within the cache as time progresses (block 14, storing a sting of

instructions is stored in the trace cache reads on this limitation).


As to claim 16, Hironaka discloses a method comprising: filling an array with

instruction cache (ICache) cache lines mixed with trace cache (TCache) cache lines

(Fig. 11 Ref. 30) where an allocated proportion of ICache cache lines to TCache cache

lines is dynamically changing with time (Fig. 14) wherein neither the ICache portion nor

the TCache portion is looked-up when the TCache portion is supplying instructions

(blocks 19, 20, and 147, executing series of instruction strings, "pseudo basic block" in a

trace cache is read on this limitation since if there a trace cache hit, traced instructions

in the trace cache are continuously accessed in a string fashion) and selecting the

TCache or the ICache portion based on an address of the next instruction (Fig. 13, hit

judgment circuit ) and using an instruction indexing logic to select some instructions

wherein the indexing logic is not used for either the ICache portion or TCache portion

when the Tcache portion is supplying instructions (blocks 19, 20, and 147, executing

series of instruction strings, "pseudo basic block" in a trace cache is read on this

limitation since if there a trace cache hit, traced instructions in the trace cache are

continuously accessed in a string fashion without using any indexing logic however if

there is a trace cache miss, instruction is fetched from a instruction cache utilizing a

fetch address).

As to claim 17, Hironaka further discloses using an address of a next instruction

when an end of a cache line is reached to determine use of the ICache cache lines or

the TCache cache lines (Fig. 13).


As to claim 18, Hironaka further discloses searching both the ICache cache lines

and the TCache cache lines when an address is a result of a branch target (Fig. 13

judgment circuit and Fig. 14).


As to claim 19, Hironaka further discloses using the TCache cache lines when an

address is found in the TCache cache lines (Fig. 13 judgment circuit).


As to claim 20, Hironaka further discloses using the ICache cache lines when the

address is found in the ICache cache lines and not in the TCache cache lines (Fig. 13

judgment circuit).


As to claim 29, Hironaka further discloses wherein the !Cache portion is

looked-up using the indexing logic when the TCache portion is not supplying

instructions (block 20).


**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.      Claims 6-8 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Hironaka et al. (Hironaka) US Patent Pub. No. 2004/0088489 in view of Takashima

et al. (Takashima) U.S. Patent 6,463,509.

As to claim 6, Hironaka discloses a system, comprising: a processor (Fig. 1 Ref.

1); a cache having in one array both an instruction cache (ICache) portion (Fig. 11 Ref.

30 and Fig. 14) and a trace cache (TCache) portion (Fig. 11 Ref. 30),  wherein a line

TCache portion is looked-up when the TCache portion is supplying instructions (blocks

19, 20, and 147, executing series of instruction strings, "pseudo basic block" in a trace

cache is read on this limitation since if there a trace cache hit, traced instructions in the

trace cache are continuously accessed in a string fashion) and an instruction indexing

logic, wherein the indexing logic is not used for either the ICache portion or TCache

portion when the Tcache portion is supplying instructions (block 20, executing series of

instruction strings, "pseudo basic block" in a trace cache is read on this limitation since if

there a trace cache hit, traced instructions in the trace cache are continuously accessed

in a string fashion without using any indexing logic however if there is a trace cache

miss, instruction is fetched from a instruction cache utilizing fetch address).

However, Hironaka does not specifically disclose at least one antenna to receive

modulated signals and supply a signal to the processor.

Takashima discloses at least one antenna to receive modulated signals and supply a signal to the processor (Fig. 25 and col. 7 line 30 thru col. 8 line 6-4) for the purpose of utilizing in the latest technology thereby increase throughput and more marketable.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate at least one antenna to receive modulated signals and supply a signal to the processor as shown in Takashima into the invention of Hironaka for the advantages stated above

As to claim 7, Hironaka and Takashima disclose the invention as claimed in the above. Hironaka further discloses the TCache portion is further indexed when the processor takes a branch, a jump, a call or a return (Fig. 11 Ref. 31).

As to claim 8, Hironaka and Takashima disclose the invention as claimed in the above. Hironaka further discloses including an indexing logic where the ICache portion is looked-up when the TCache portion is not supplying instructions (Fig. 13, hit judgment circuit).

As to claim 22, Hironaka and Takashima disclose the invention as claimed in the above. Takashima further discloses wherein the at least one antenna comprises a Radio Frequency (RF) transceiver (Fig. 25 Refs. 93 and 94).

As to claim 23, Hironaka and Takashima disclose the invention as claimed in the

above. Takashima further discloses a control circuit to control the storage and retrieval

of data words stored in the cache (Fig. 13, hit judgment circuit).


As to claim 24, Hironaka and Takashima disclose the invention as claimed in the

above. Hironaka further discloses wherein the TCache line size is a multiple of the

ICache line size (block 20, fetch from Icache when there is a Tcache miss reads on this

limitation).


As to claim 25, Hironaka and Takashima disclose the invention as claimed in the

above. Hironaka further discloses wherein the !Cache and TCache portions may

migrate within the cache as time progresses (block 14, storing a sting of instructions is

stored in the trace cache reads on this limitation).


### Conclusion

1.    The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.   See attached PTO-892.


2.    A shortened statutory period for response to this action is set to expire 3 (three)

months and 0 (zero) days from the mail date of this letter.  Failure to respond within the

period for response will result in **ABANDONMENT** of the application (see 35 USC 133,

MPEP 710.02, 710.02(b)).

3.    When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections.    See 37 C.F.R. ' 1.111(c).

4.    When responding to the office action, Applicants are advised to provide the

examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

5.    Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Hong C Kim whose telephone number is (571) 272-

4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should

be directed to the TC 2100 whose telephone number is (571) 272-2100.

6.      Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system.  Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).


7.      **Any response to this action should be mailed to:**

> Commissioner of Patents
> P.O. Box 1450
> Alexandria, VA 22313-1450
>
> **or faxed to TC-2100:**
> (703) 872-9306
>
> Hand-delivered responses should be brought to the Customer Service
> Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).


H Kim
Primary Patent Examiner
January 6, 2007